Amendments to the Claims:
This listing of claims will replace all prior versions, and listings of claims in the application:
Listing of Claims:

147. (Amended) A method for operating a computing system comprises:

fetching a first 256 bit-wide frame of instructions from an instruction memory, the first frame of instructions comprising up to eight 32 bit-wide instructions, each 32-bit wide instruction comprising 31 contiguous bits of instruction data and a one bit wide grouping bit, wherein grouping bits of the 32 bit-wide instructions are indicative of groups of instructions from the first frame of instructions, wherein the groups of instructions ~~comprises~~ comprise at least one group of instructions and ~~comprises~~ comprise at most eight groups of individual instructions, wherein a group of instructions are issued separately from other groups of instructions within the first frame of instructions, wherein groups of instructions are issued from left-to-right from the first frame of instructions, and wherein instructions within a group of instructions are issued in parallel;

issuing instructions in a first group of instructions from the first frame of instructions to functional units appropriate for the instructions in the first group of instructions in response to grouping bits of the instructions in the first group of instructions and in response to a mapping of the instructions in the first group of instructions to functional units, wherein the mapping is determined in response to at least a portion of instruction data in each instruction in the first group of instructions from the first frame of instructions;

fetching a second 256 bit-wide frame of instructions from the instruction memory, the second frame of instructions comprising up to eight 32 bit-wide instructions, each 32-bit wide instruction comprising 31 contiguous bits of instruction data and a one bit wide grouping bit, wherein grouping bits of the 32 bit-wide instructions are indicative of groups of instructions from the second frame of instructions, wherein the groups of instructions ~~comprises~~ comprise at least one group of instructions and ~~comprises~~ comprise at most eight groups of individual instructions, wherein a group of instructions are issued separately from other groups of instructions within the second frame of instructions, wherein groups of instructions are issued from left-to-right from the second frame of instructions, and wherein instructions within a group of instructions are issued in parallel; and

issuing instructions in a first group of instructions from the second frame of instructions to functional units appropriate for the instructions in the first group of instructions in response to grouping bits of the instructions in the first group of instructions and in response to a mapping of the instructions in the first group of instructions to functional units, wherein the mapping is determined in response to at least a portion of instruction data in each instruction in the first group of instructions from the second frame of instructions;

wherein instructions from the first 256 bit-wide frame of instructions are issued before fetching the second 256 bit-wide frame of instructions from the instruction memory; and

wherein the ~~groups of~~ grouping bits of the 32 bit-wide instructions from the first frame of instructions and the ~~groups of~~ grouping bits of the 32 bit-wide instructions from the second frame of instructions are ~~specified~~ specifiable at compile time.

2 148. (Original) The method of claim 147 wherein the first 256 bit-wide frame of instructions comprises less then eight 32 bit-wide instructions.

3 149. (Original) The method of claim 147 further comprising:
issuing instructions in a second group of instructions from the first frame of instructions to functional units appropriate for the instructions in the second group of instructions in response to grouping bits of the instructions in the second group of instructions and in response to a mapping of the instructions in the second group of instructions to functional units, wherein the mapping is determined in response to a portion of instruction data in each instruction in the second group of instructions from the first frame of instructions.

4 150. (Original) The method of claim 149 wherein a functional unit appropriate for an instruction in the second group of instructions from the first frame of instruction comprises a floating point unit.

5 151. (Original) The method of claim 150 wherein the second group of instructions from the first frame of instructions includes a floating point instruction.

6 152. (Original) The method of claim 147 wherein the first 256 bit-wide frame of instructions comprises exactly eight 32 bit-wide instructions.

7 153. (Original) The method of claim 152 further comprising:
issuing instructions in a second group of instructions from the second frame of instructions to functional units appropriate for the instructions in the second group of instructions in response to grouping bits of the instructions in the second group of instructions and in response to a mapping of the instructions in the second group of instructions to functional units, wherein the mapping is determined in response to at least a portion of instruction data in each instruction in the second group of instructions from the second frame of instructions.

8 154. (Original) The method of claim 147 wherein three groups of instructions are packed within the first 256 bit-wide frame of instructions thereby reducing instruction code size.

9 155. (Original) The method of claim 154 wherein issuing instructions in a first group of instructions from the first frame of instructions further comprises decoding the instructions in the first group of instructions before issuance to functional units appropriate for the instructions in the first group of instructions from the first frame of instructions.

10 156. (Original) The method of claim 147 wherein four groups of instructions are packed within the first 256 bit-wide frame of instructions thereby reducing a number of no-operations within the first 256 bit-wide frame of instructions.

11 10
~~157.~~ (Original) The method of claim ~~156~~ wherein groups of instructions are not split across the first 256 bit-wide frame of instructions and the second 256 bit-wide frame of instructions.

12 10
~~158.~~ (Amended) The method of claim ~~156~~ wherein the ~~groups of~~ grouping bits of the 32 bit-wide instructions from the first frame of instructions and the ~~groups of~~ grouping bits of the 32 bit-wide instructions from the second frame of instructions are specified at compile time in response to data dependency checking of the instructions in the first frame of instructions and in response to data dependency checking of the instructions in the second frame of instructions.

13 1
~~159.~~ (Original) The method of claim ~~147~~ wherein the instructions in the first instruction frame are stored in little-endian format.

14 13
~~160.~~ (Original) The method of claim ~~159~~ wherein the functional units appropriate for the instructions in the first group of instructions in the first frame of instructions are selected from a group of eight functional units.

15 1
~~161.~~ (Amended) The method of claim ~~147~~
wherein the groups of instructions from the first frame of instructions ~~comprises~~ comprise the first group of instructions, a second group of instructions, and a third group of instructions;

wherein instructions grouped as the second group of instructions are to be issued in parallel to appropriate functional units before instructions grouped as the third group of instructions are to be issued in parallel.

16 15
~~162.~~ (Original) The method of claim ~~161~~
wherein the first group of instructions comprises two instructions to be issued in parallel;

wherein the second group of instructions comprises three instructions to be issued in parallel; and

wherein the third group of instructions comprises three instructions to be issued in parallel.

17 15
~~163.~~ (Original) The method of claim ~~161~~
wherein the groups of instructions from the first frame of instructions also comprise a fourth group of instructions;

wherein instructions grouped as the third group of instructions are to be issued in parallel to appropriate functional units before instructions grouped as the fourth group of instructions are to be issued in parallel;

wherein the third group of instructions comprises two instructions to be issued in parallel; and

wherein the fourth group of instructions comprises two instructions to be issued in parallel.

18 1
164. (Original) The method of claim 147 wherein the first group of instructions from the first frame of instructions includes two add instructions that are issued in parallel to functional units appropriate for the two add instructions.

19 18
165. (Original) The method of claim 164 wherein the functional units include two arithmetic logic units.

20 18
166. (Original) The method of claim 164 wherein the first group of instructions from the first frame of instructions also includes a load instruction.

21 1
167. (Original) The method of claim 147 wherein an instruction in the first group of instructions from the first frame of instructions operates upon registers.

22 21
168. (Original) The method of claim 167 wherein an instructions from the first frame of instructions comprises a branch instruction.

23
169. (Amended) A processor comprises:

a plurality of functional units;

an instruction memory configured to store a first 256-bit wide frame of instructions, the first frame of instructions comprising up to eight 32 bit-wide instructions, each 32-bit wide instruction comprising 31 contiguous bits of instruction data and a one bit wide grouping bit, wherein grouping bits of the 32 bit-wide instructions are indicative of variable length groups of instructions from the first frame of instructions, wherein the variable length groups of instructions ~~comprises~~ comprise at least one group of instructions and ~~comprises~~ comprise at most eight groups of individual instructions, wherein a group of instructions are dispatched separately from other groups of instructions within the first frame of instructions, wherein groups of instructions are dispatched from left-to-right from the first frame of instructions, and wherein instructions within a group of instructions are dispatched in parallel; and

an instruction dispatching unit coupled to the instruction memory and the plurality of functional units, the instruction dispatching unit configured to dispatch instructions in a first group of instructions from the first frame of instructions to functional units appropriate for the instructions in the first group of instructions in response to grouping bits of the instructions in the first group of instructions and in response to a mapping of the instructions in the first group of instructions to functional units, wherein the mapping is determined in response to at least a portion of instruction data in each instruction in the first group of instructions from the first frame of instructions; and

wherein the grouping bits ~~groups~~ of the 32 bit-wide instructions from the first frame of instructions are ~~determined~~ determinable at compile time.

24 23
~~170.~~ (Amended) The processor of claim ~~169~~ wherein the instruction memory is also configured to store a second 256 bit-wide frame of instructions, the second frame of instructions comprising up to eight 32 bit-wide instructions, each 32-bit wide instruction comprising 31 contiguous bits of instruction data and a one bit wide grouping bit, wherein grouping bits of the 32 bit-wide instructions are indicative of variable length groups of instructions from the second frame of instructions, wherein the variable length groups of instructions ~~comprises~~ comprise at least one group of instructions and ~~comprises~~ comprise at most eight groups of individual instructions, wherein a group of instructions are dispatched separately from other groups of instructions within the second frame of instructions, wherein groups of instructions are dispatched from left-to-right from the second frame of instructions, and wherein instructions within a group of instructions are dispatched in parallel;

wherein the instruction dispatching unit is also configured to dispatch instructions in a first group of instructions from the second frame of instructions to functional units appropriate for the instructions in the first group of instructions in response to grouping bits of the instructions in the first group of instructions and in response to a mapping of the instructions in the first group of instructions to functional units, wherein the mapping is determined in response to at least a portion of instruction data in each instruction in the first group of instructions from the second frame of instructions; and

wherein the first group of instructions from the first 256-bit wide frame of instructions are dispatched before the first group of instruction in the second 256 bit-wide frame of instructions.

25 24
~~171.~~ (Original) The processor of claim ~~170~~ wherein the instruction dispatching unit is also configured to dispatch instructions in a second group of instructions from the first frame of instructions to functional units appropriate for the instructions in the second group of instructions in response to grouping bits of the instructions in the second group of instructions and in response to a mapping of the instructions in the second group of instructions to functional units, wherein the mapping is determined in response to at least a portion of instruction data in each instruction in the second group of instructions from the first frame of instructions.

26 25
~~172.~~ (Original) The processor of claim ~~171~~ wherein the first 256 bit-wide frame of instructions comprises less than eight 32 bit-wide instructions and a no operation.

27 23
~~173.~~ (Original) The processor of claim ~~169~~ wherein the plurality of functional units comprises a functional unit configured to perform floating-point operations.

28 27
~~174.~~ (Original) The processor of claim ~~173~~ wherein an instruction in the first frame of instructions comprises a floating point instruction.

29 ~~175.~~ (Original) The processor of claim 23 ~~169~~ wherein the plurality of functional units also comprises a functional unit configured to perform a load operation and a store operation.

30 ~~176.~~ (Original) The processor of claim 29 ~~175~~ wherein the plurality of functional units also comprises a functional unit configured to perform branch instructions.

31 ~~177.~~ (Original) The processor of claim 30 ~~176~~ wherein the first 256 bit-wide frame of instructions comprises exactly eight 32 bit-wide instructions.

32 ~~178.~~ (Original) The processor of claim 23 ~~169~~ wherein at least three groups of instructions are packed within the first 256 bit-wide frame of instructions thereby saving memory space.

33 ~~179.~~ (Original) The processor of claim 32 ~~178~~ wherein the instruction dispatching unit is also configured to fetch the first frame of instructions and configured to decode the instructions in the first group of instructions before dispatch to functional units appropriate for the instructions in the first group of instructions from the first frame of instructions.

34 ~~180.~~ (Original) The processor of claim 23 ~~169~~ wherein groups of instructions to be dispatched in parallel are not split across frames of instructions.

35 ~~181.~~ (Original) The processor of claim 34 ~~180~~ wherein four groups of instructions are packed within the first 256 bit-wide frame of instructions thereby reducing memory bandwidth.

36 ~~182.~~ (Amended) The processor of claim 34 ~~180~~ wherein the grouping bits ~~groups~~ of the 32 bit-wide instructions from the first frame of instructions are ~~specified~~ determined at compile time ~~by the grouping bits of the instructions in the first frame of instructions~~ in response to data dependency checking of the instructions in the first frame of instructions.

37 ~~183.~~ (Original) The processor of claim 23 ~~169~~ wherein the functional units appropriate for the instructions in the first group of instructions in the first frame of instructions are selected from a group of eight functional units.

38 ~~184.~~ (Original) The processor of claim 37 ~~183~~ wherein the instructions in the first instruction frame are stored in little-endian format.

39 ~~185.~~ (Amended) The processor of claim 23 ~~169~~

wherein the groups of instructions from the first frame of instructions ~~comprises~~ comprise the first group of instructions, a second group of instructions, and a third group of instructions;

wherein the instruction dispatching unit is also configured to dispatch instructions in a second group of instructions from the first frame of instructions to functional units appropriate for the instructions in the second group of instructions in response to grouping bits of the instructions in the second group of instructions and in response to a mapping of the instructions in the second group of instructions to functional units, wherein the mapping is determined in response to at least a portion of instruction data in each instruction in the second group of instructions from the first frame of instructions; and

wherein the instruction dispatching unit is also configured to dispatch instructions grouped as the first group of instructions in parallel to appropriate functional units before dispatching instructions grouped as the second group of instructions in parallel.

40 39
~~186.~~ (Original) The processor of claim ~~185~~

wherein the first group of instructions comprises two instructions to be dispatched in parallel;

wherein the second group of instructions comprises three instructions to be dispatched in parallel; and

wherein the third group of instructions comprises three instructions to be dispatched in parallel.

41 39
~~187.~~ (Original) The processor of claim ~~185~~

wherein the groups of instructions from the first frame of instructions also comprise a fourth group of instructions;

wherein the instruction dispatching unit is also configured to dispatch instructions in a third group of instructions from the first frame of instructions to functional units appropriate for the instructions in the third group of instructions in response to grouping bits of the instructions in the third group of instructions and in response to a mapping of the instructions in the third group of instructions to functional units, wherein the mapping is determined in response to at least a portion of instruction data in each instruction in the third group of instructions from the first frame of instructions;

wherein the instruction dispatching unit is also configured to dispatch instructions grouped as the second group of instructions in parallel to appropriate functional units before dispatching instructions grouped as the third group of instructions in parallel;

wherein the third group of instructions comprises two instructions to be dispatched in parallel; and

wherein the fourth group of instructions comprises two instructions to be dispatched in parallel.

42 23
~~188.~~ (Original) The processor of claim ~~169~~ wherein the plurality of functional units include functional units configured to perform arithmetic and logic operations.

43 42
189. (Original) The processor of claim 188 wherein an instruction of the first group of instructions from the first frame of instructions comprises a load instruction.

44 42
190. (Original) The processor of claim 188 wherein the instructions of the first group from the first frame of instructions comprises two addition instructions.

45 42
191. (Original) The processor of claim 188 wherein at least one instruction in the first group of instructions from the first frame of instructions operates upon registers.

46 42
192. (Original) The processor of claim 188 wherein an instruction from the first frame of instructions comprises a branch instruction.

47
193. (Amended) An apparatus comprises:
a memory configured to store a plurality of instruction data; and
a processor coupled to the memory comprising:
a memory controller configured to receive a first set of instruction data from the memory;
a plurality of functional units;
an instruction memory configured to store a first 256-bit wide frame of instructions in response to the first set of instruction data from the memory, the first frame of instructions comprising up to eight 32 bit-wide instructions, each 32-bit wide instruction comprising 31 contiguous bits of instruction data and a one bit wide grouping bit, wherein grouping bits of the 32 bit-wide instructions are indicative of groups of instructions of variable lengths from the first frame of instructions, wherein the groups of instructions ~~comprises~~ comprise at least one group of instructions and ~~comprises~~ comprise at most eight groups of instructions, wherein a number of instructions in the groups of instructions comprises at least one instruction and up to eight instructions ; , wherein a group of instructions are dispatched separately from other groups of instructions within the first frame of instructions, wherein groups of instructions are dispatched from left-to-right from the first frame of instructions, and wherein instructions within a group of instructions are dispatched in parallel; and
an instruction dispatching unit coupled to the instruction memory and coupled to the plurality of functional units, the instruction dispatching unit configured to fetch the first frame of instructions from the instruction memory and configured to dispatch instructions in a first group of instructions from the first frame of instructions to functional units appropriate for the instructions in the first group of instructions in response to grouping bits of the instructions in the first group of instructions and in response to a mapping of the instructions in the first group of instructions to appropriate functional units, wherein the mapping is determined in response to at least a portion of instruction data in each instruction in the first group of instructions from the first frame of instructions;
wherein the ~~groups~~ grouping bits of the instructions in the first group of instructions from the first frame of instructions are ~~determined~~ determinable at compile time.

48 47
194. (Amended) The apparatus of claim 193

wherein the memory controller is configured to receive a second set of instruction data from the memory;

wherein the instruction memory is also configured to store a second 256-bit wide frame of instructions in response to the second set of instruction data from the memory, the second frame of instructions comprising up to eight 32 bit-wide instructions, each 32-bit wide instruction comprising 31 contiguous bits of instruction data and a one bit wide grouping bit, wherein grouping bits of the 32 bit-wide instructions are indicative of groups of instructions of variable lengths from the second frame of instructions, wherein the groups of instructions ~~comprises~~ comprise at least one group of instructions and ~~comprises~~ comprise at most eight groups of instructions, wherein a number of instructions in the groups of instructions comprises at least one instruction and up to eight instructions ~~;~~ , wherein a group of instructions are dispatched separately from other groups of instructions within the second frame of instructions, wherein groups of instructions are dispatched from left-to-right from the first frame of instructions, and wherein instructions within a group of instructions are dispatched in parallel; and

wherein the instruction dispatching unit is also configured to fetch the second frame of instructions from the instruction memory and configured to dispatch instructions in a first group of instructions from the second frame of instructions to functional units appropriate for the instructions in the first group of instructions in response to grouping bits of the instructions in the first group of instructions and in response to a mapping of the instructions in the first group of instructions to appropriate functional units, wherein the mapping is determined in response to at least a portion of instruction data in each instruction in the first group of instructions from the second frame of instructions;

wherein the ~~first group~~ grouping bits of the instructions in the first group of instructions from the first 256-bit wide frame of instructions and the ~~first group~~ grouping bits of the instructions in the first group of instructions from ~~in~~ the second 256 bit-wide frame of instructions are ~~determined~~ determined at compile time.

49 48
~~193.~~ (Original) The apparatus of claim ~~194~~ wherein the instruction dispatching unit is also configured to dispatch instructions in a second group of instructions from the first frame of instructions to functional units appropriate for the instructions in the second group of instructions in response to grouping bits of the instructions in the second group of instructions and in response to a mapping of the instructions in the second group of instructions to appropriate functional units, wherein the mapping is determined in response to at least a portion of instruction data in each instruction in the second group of instructions from the first frame of instructions.

50 48
~~196.~~ (Original) The apparatus of claim ~~194~~ wherein the first 256 bit-wide frame of instructions comprises a no operation.

51 47
~~197.~~ (Amended) The apparatus of claim ~~193~~ wherein the plurality of functional units ~~comprises~~ comprise eight functional units including a floating-point unit.

52 198. (Original) The apparatus of claim 197 wherein an instruction in a group of instructions from the first frame of instructions comprises a floating point instruction.

53 199. (Original) The apparatus of claim 198 wherein the plurality of functional units also includes a functional unit configured to perform a load operation.

54 200. (Original) The apparatus of claim 197 wherein the plurality of functional units also includes a branch unit.

55 201. (Original) The apparatus of claim 200 wherein the first 256 bit-wide frame of instructions comprises exactly eight 32 bit-wide instructions.

56 202. (Original) The apparatus of claim 193 wherein more than two groups of instructions are packed within the first 256 bit-wide frame of instructions thereby reducing instruction code size.

57 203. (Original) The apparatus of claim 202 wherein the instruction dispatching unit is also configured to decode the instructions in the first group of instructions before dispatch to the appropriate functional units.

58 204. (Original) The apparatus of claim 203 wherein groups of instructions to be dispatched in parallel are not split across frames of instructions.

59 205. (Amended) The apparatus of claim 202 wherein the ~~groups~~ grouping bits of the instructions in the first group of instructions from the first frame of instructions are specified at compile time ~~by the grouping bits of the instructions in the first frame of instructions~~ in response to data dependency checking of the instructions in the first group of instructions from the first frame of instructions.

60 206. (Original) The apparatus of claim 202 wherein the instructions in the first instruction frame are stored in little-endian format.

61 207. (Amended) The apparatus of claim 193

wherein the groups of instructions from the first frame of instructions ~~comprises~~ comprise the first group of instructions, a second group of instructions, and a third group of instructions; and

wherein a number of instructions in the first group of instructions is different from a number of instructions in the second group of instructions.

62 208. (Original) The apparatus of claim 207

wherein the groups of instructions from the first frame of instructions also comprise a fourth group of instructions; and

wherein a number of instructions in the first group of instructions is different from a number of instructions in the fourth group of instructions.

63 61
~~209.~~ (Original) The apparatus of claim ~~207~~ wherein the plurality of functional units includes at least one arithmetic logic unit.

64 42
~~210.~~ (Original) The apparatus of claim ~~188~~
wherein the plurality of functional units includes at least two arithmetic logic units; and

wherein the first group of instructions from the first frame of instructions comprises two addition instructions.

65 64
~~211.~~ (Amended) The apparatus of claim ~~210~~ wherein the first group of instructions from the first frame of instructions also ~~comprises~~ comprise a load instruction.

66 65
~~212.~~ (Original) The apparatus of claim ~~211~~ wherein the two addition instructions operate upon registers.

67 47
~~213.~~ (Original) The apparatus of claim ~~193~~
wherein a number of instructions in the first group of instructions is equal to a number of instructions in the second group of instructions.

68 67
~~214.~~ (Original) The apparatus of claim ~~213~~ wherein the number of instructions in the first group of instructions is exactly one instruction.

69 47
~~215.~~ (Original) The apparatus of claim ~~193~~ wherein the right-most instruction in the first frame of instructions is configured to store a branch operation.

70
~~216.~~ (Amended) An instruction memory comprises:

a first 256-bit wide frame of instructions comprising eight 32 bit-wide instructions, each 32-bit wide instruction comprising 31 contiguous bits of instruction data and a one bit wide grouping bit, wherein grouping bits of the 32 bit-wide instructions are indicative of groups of variable ~~number~~ numbers of instructions from the first frame of instructions, wherein the first frame of instructions ~~comprises~~ comprise at least one group of instructions and ~~comprises~~ comprise at most eight groups of instructions, wherein a number of instructions in the groups of instructions comprises at least one instruction and up to eight instructions ; ,wherein a group of instructions are dispatched serially from left-to-right within the first frame of instructions, and wherein instructions within a group of instructions are dispatched in parallel; and

a second 256-bit wide frame of instructions comprising eight 32 bit-wide instructions, each 32-bit wide instruction comprising 31 contiguous bits of instruction data and a one bit wide grouping bit, wherein grouping bits of the 32 bit-wide instructions are indicative of groups of variable ~~number~~ numbers of instructions from the second frame of instructions,

wherein the second frame of instructions ~~comprises~~ comprise at least one group of instructions and ~~comprises~~ comprise at most eight groups of instructions, wherein a number of instructions in the groups of instructions comprises at least one instruction and up to eight instructions ~~;~~, wherein a group of instructions are dispatched serially from left-to-right within the second frame of instructions, and wherein instructions within a group of instructions are dispatched in parallel;

wherein a first group of instructions from the first frame of instructions are ~~fetched and~~ dispatched to functional units appropriate for instructions in the first group in response to grouping bits of the instructions in the first group of instructions;

wherein a second group of instructions from the first frame of instructions are ~~fetched and~~ dispatched to functional units appropriate for instructions in the second group in response to grouping bits of the instructions in the second group of instructions;

wherein a first group of instructions from the second frame of instructions are ~~fetched and~~ dispatched to functional units appropriate for instructions in the first group in response to grouping bits of the instructions in the first group of instructions from the second frame of instructions; and

wherein the grouping bits of the instructions in the first frame of instructions and the grouping bits of the instructions in the second frame of instructions are determined at a time other than run-time.

71 70

~~217.~~ (Amended) The instruction memory of claim ~~216~~ wherein the first group of instructions from the second frame of instructions are ~~fetched~~ dispatched only after all instructions in the first frame of instructions are dispatched.

72 71

~~218.~~ (Amended) The instruction memory of claim ~~217~~ wherein the ~~first group~~ grouping bits of the instructions from the first frame of instructions and the ~~first group~~ grouping bits of the instructions ~~in~~ from the second frame of instructions are determined at compile time.

73 72

~~219.~~ (Original) The instruction memory of claim ~~218~~ wherein the first group of instructions from the first frame of instructions are dispatched in response to a mapping of the instructions in the first group of instructions to appropriate functional units; and

wherein the mapping of the instructions is determined in response to at least a portion of instruction data in each instruction in the first group of instructions from the first frame of instructions.

74 72

~~220.~~ (Original) The instruction memory of claim ~~218~~ wherein an instruction in the first frame of instructions comprises a no-op instruction.

75 70

~~221.~~ (Original) The instruction memory of claim ~~216~~ wherein functional units appropriate for instructions in the first group of instructions in the first frame of instructions comprise eight functional units.

~~222.~~ 76 (Original) The instruction memory of claim ~~221~~ 75 wherein a functional unit appropriate for an instruction in the first frame of instructions comprises a floating point unit.

~~223.~~ 77 (Original) The instruction memory of claim ~~222~~ 76 wherein an instruction in the first frame of instructions is sent to a functional unit that performs a store operation.

~~224.~~ 78 (Original) The instruction memory of claim ~~222~~ 76 wherein a functional unit appropriate for an instruction in the first frame of instructions comprises an arithmetic logic unit.

~~225.~~ 79 (Original) The instruction memory of claim ~~224~~ 78 wherein instructions in the first group of instructions from the first frame of instructions comprise two ALU instructions.

~~226.~~ 80 (Original) The instruction memory of claim ~~225~~ 79 wherein an instruction in the second group of instructions from the first frame of instructions comprises a floating point instruction.

~~227.~~ 81 (Original) The instruction memory of claim ~~226~~ 80 wherein an instruction from the first frame of instructions comprises a branch instruction.

~~228.~~ 82 (Original) The instruction memory of claim ~~216~~ 70 wherein more than two groups of instructions are packed within the first 256 bit-wide frame of instructions thereby reducing instruction code size.

~~229.~~ 83 (Original) The instruction memory of claim ~~228~~ 82 wherein the instructions in the first group of instructions are decoded prior to dispatch to the appropriate functional units.

~~230.~~ 84 (Original) The instruction memory of claim ~~229~~ 83 wherein the instructions in the first group of instructions in the first frame of instructions are checked for data dependency at compile time.

~~231.~~ 85 (Original) The instruction memory of claim ~~229~~ 83 wherein instructions stored in the first frame of instructions and stored in the second frame of instructions are not grouped into a single group of instructions.

~~232.~~ 86 (Original) The instruction memory of claim ~~228~~ 82 wherein the instructions in the first instruction frame and the instructions in the second instruction are stored in little-endian format.

87 (~~233~~.) (Original) The instruction memory of claim 70 (~~216~~) wherein the first group of instructions and the second group of instructions are packed into the first 256 bit-wide frame of instructions to reduce a number of no-operations in the first 256 bit-wide frame of instructions.

88 (~~234~~.) (Original) The instruction memory of claim 87 (~~233~~) wherein a number of instructions in the first group of instructions is identical to a number of instructions in the second group of instructions.

89 (~~235~~.) (Original) The instruction memory of claim 88 (~~234~~)

wherein the first frame of instructions also comprise a third group of instructions; and

wherein a number of instructions in the third group of instructions comprises more than one instruction.

90 (~~236~~.) (Original) The instruction memory of claim 89 (~~235~~) wherein an instruction in the first group of instructions from the first frame of instruction specifies at least one source register and one destination register.